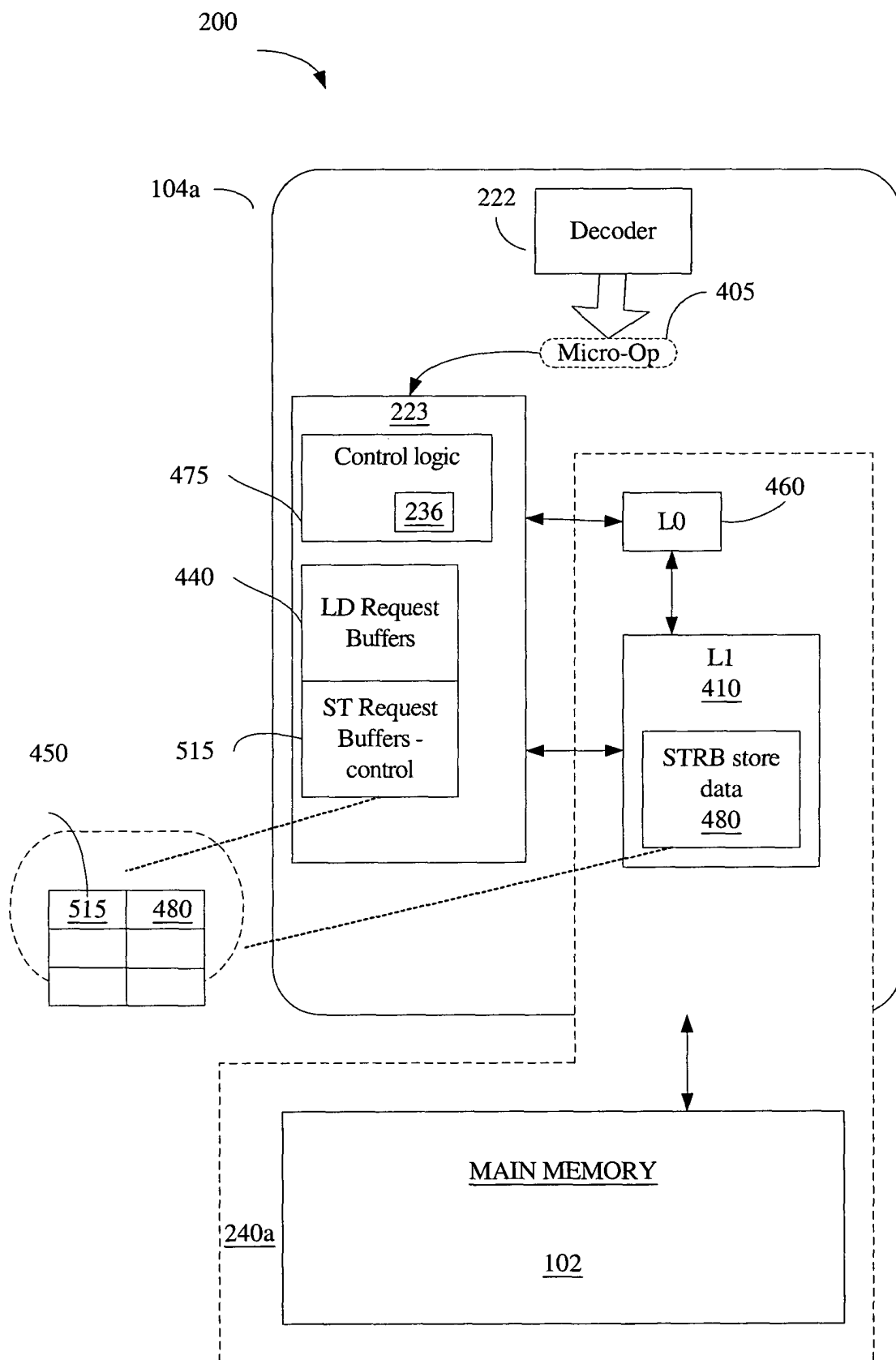
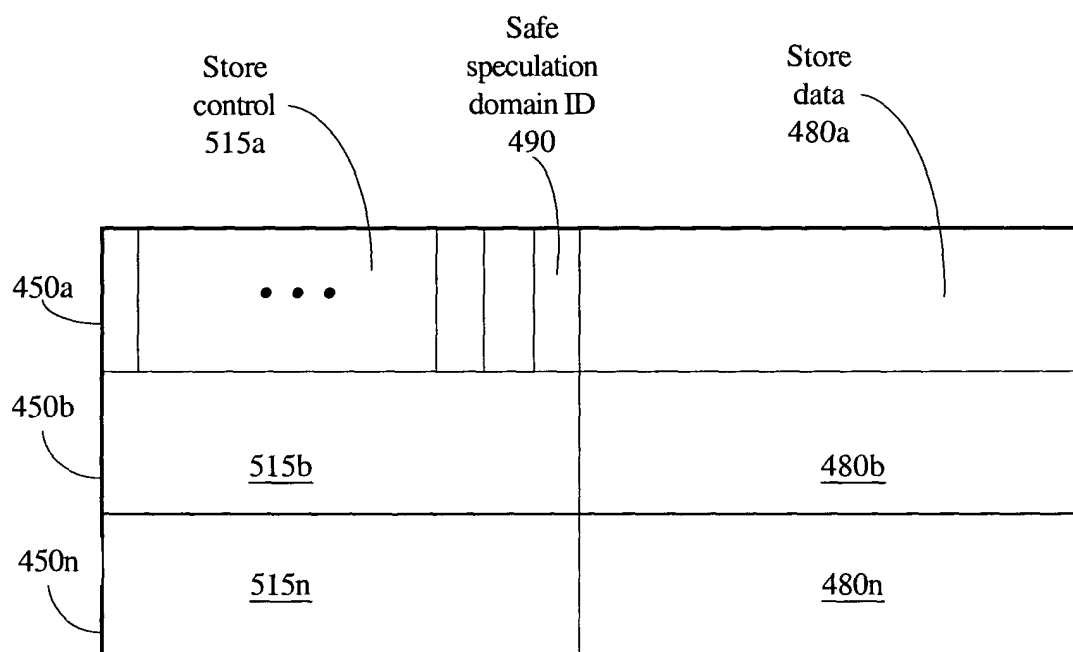


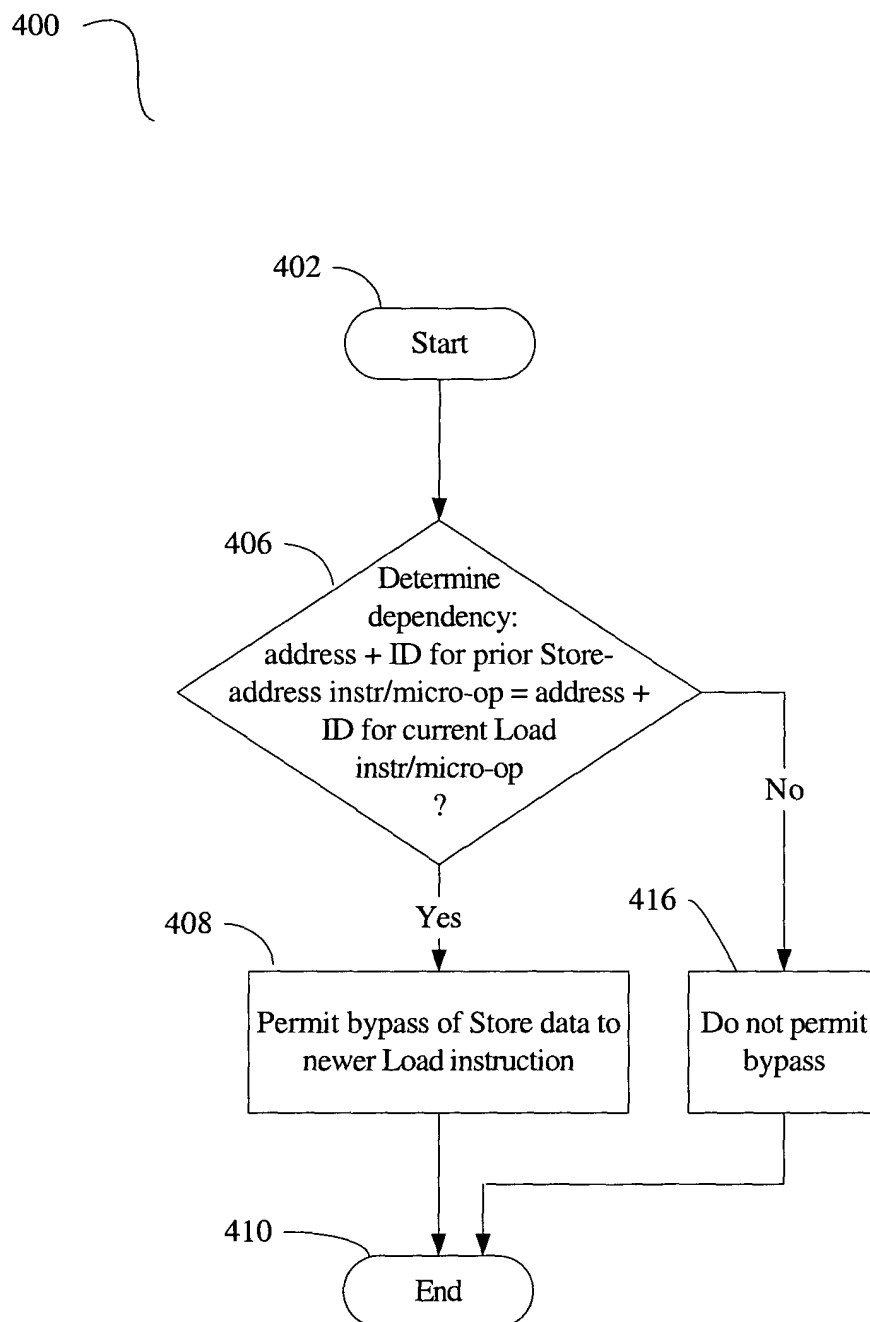
**Fig. 1**



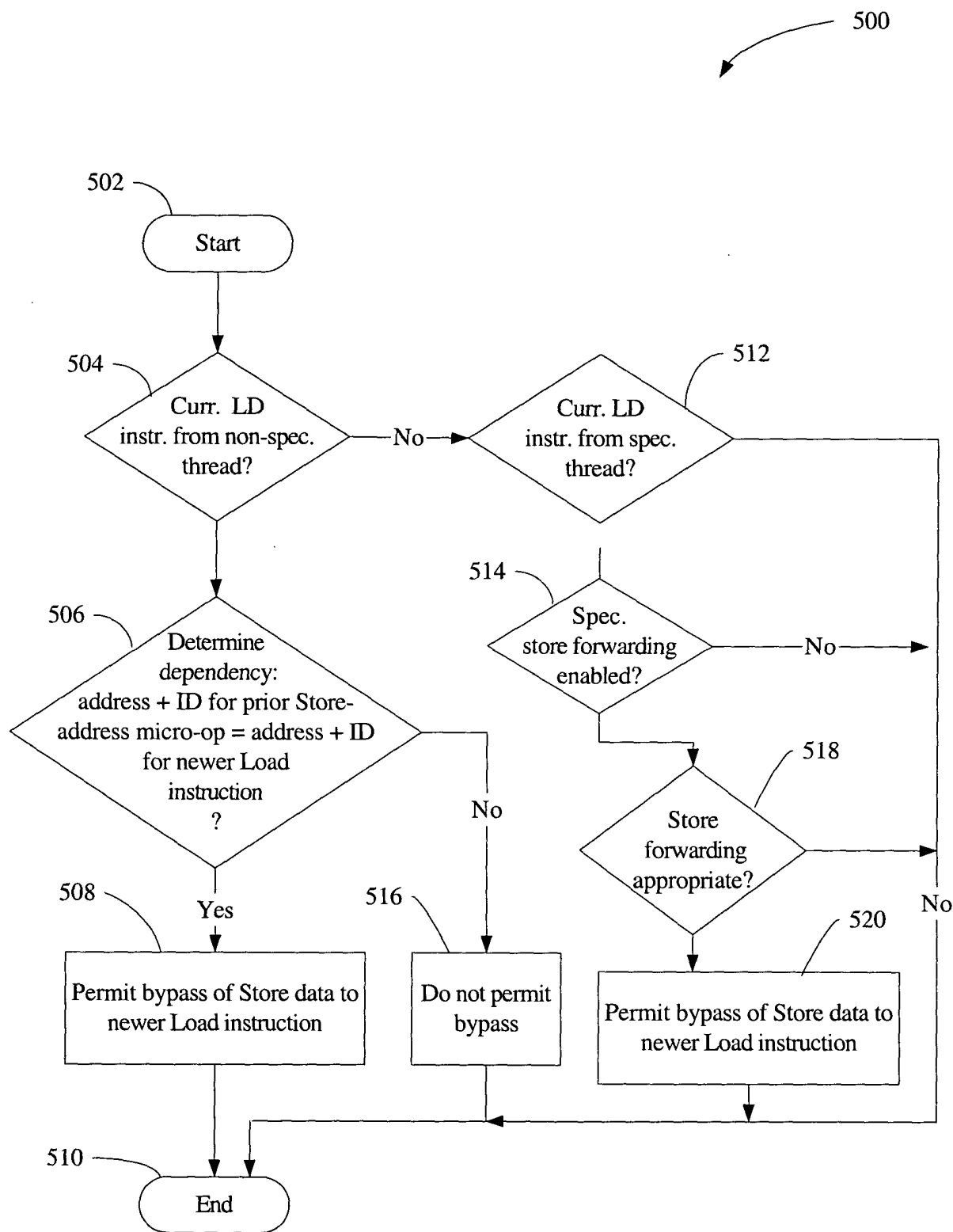
**Fig. 2**



**Fig. 3**



**Fig. 4**



**Fig. 5**

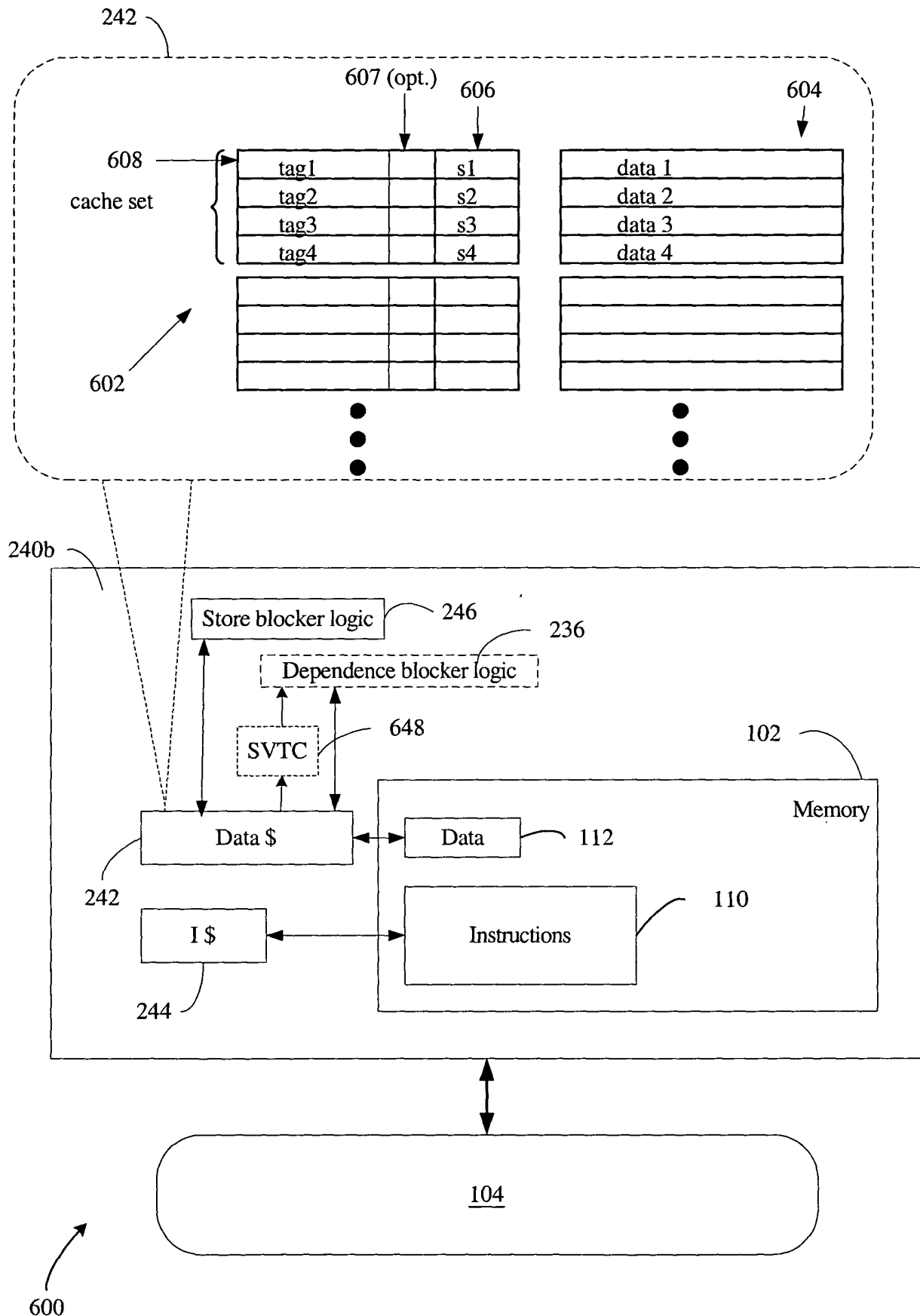
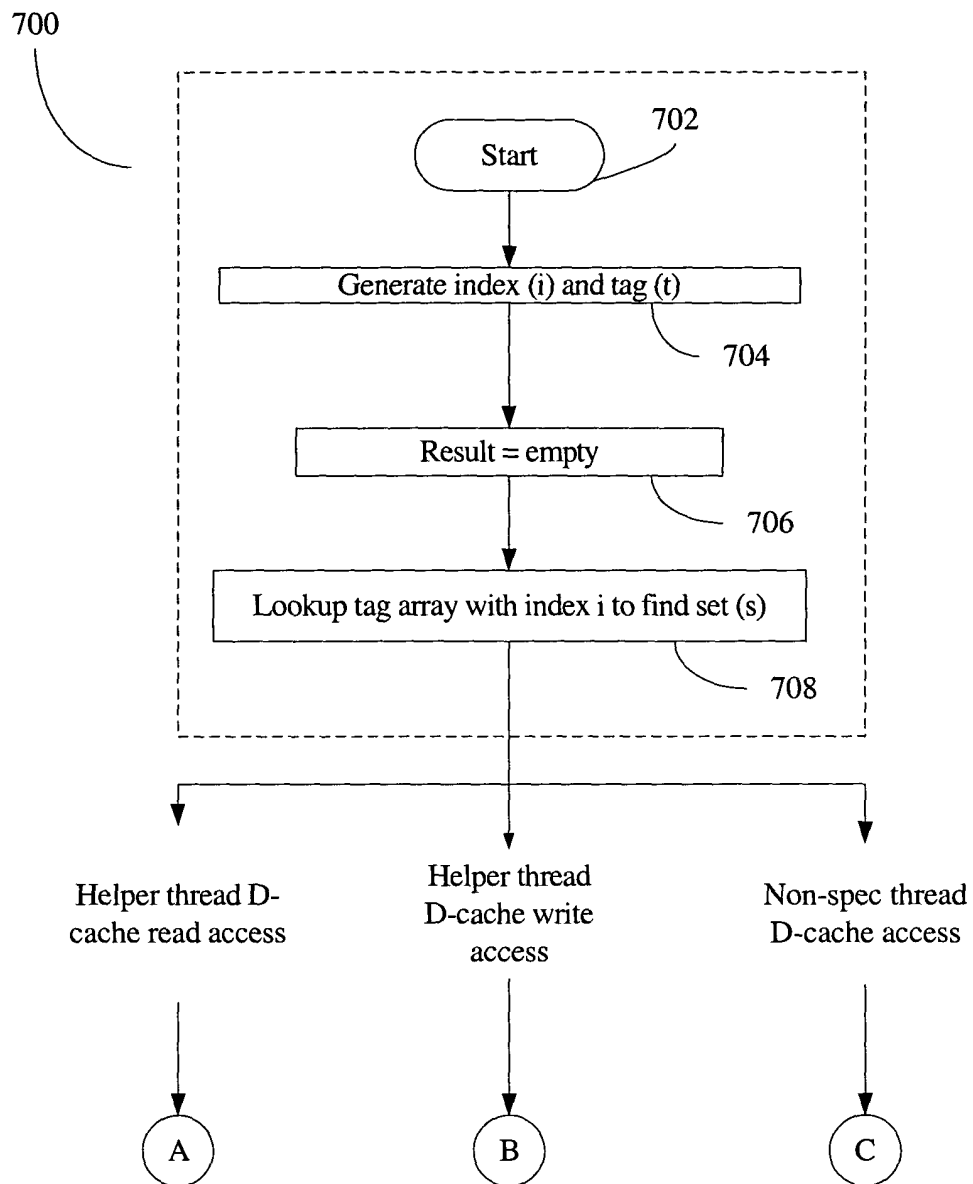


Fig. 6



**Fig. 7**

Helper thread D-  
cache read access

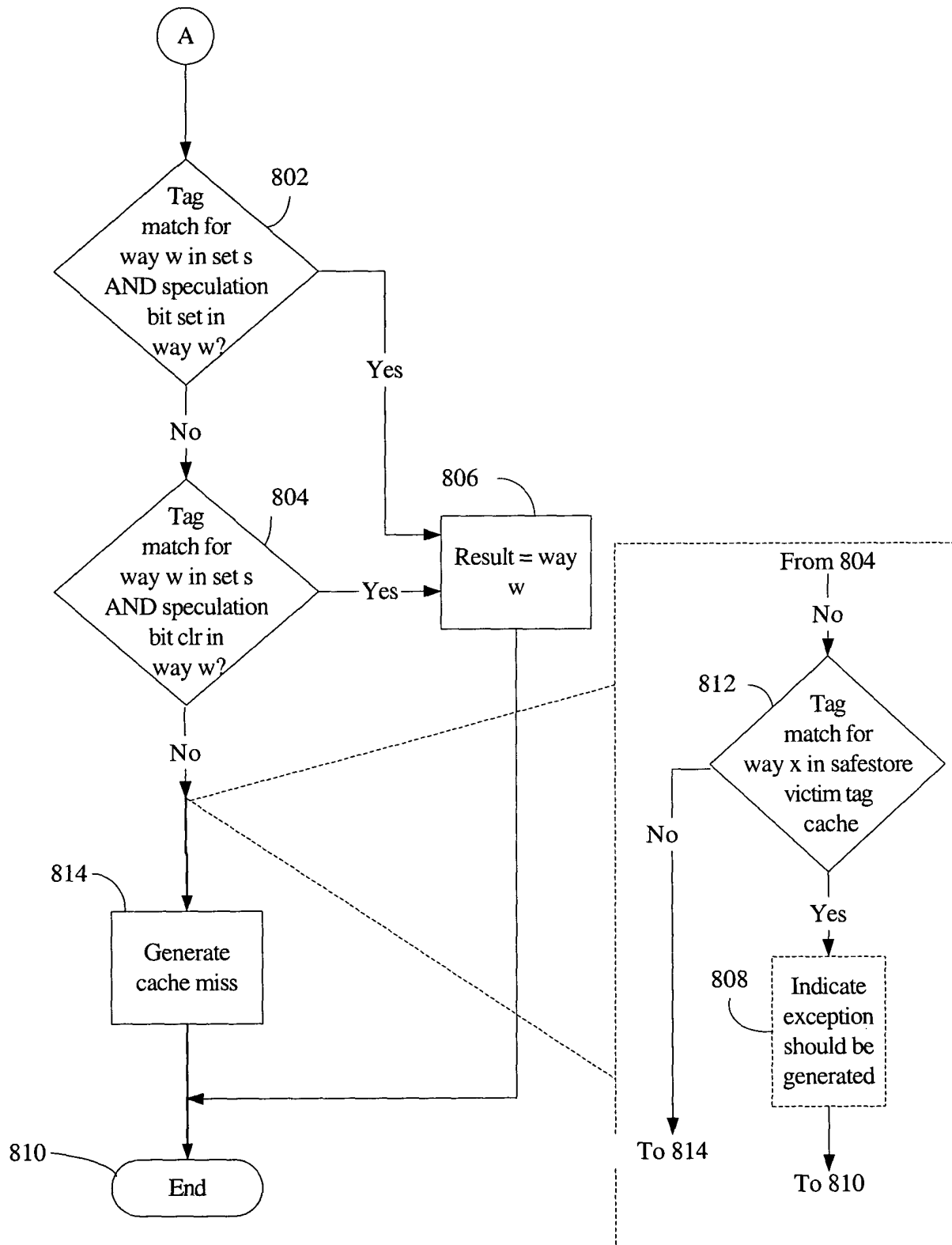
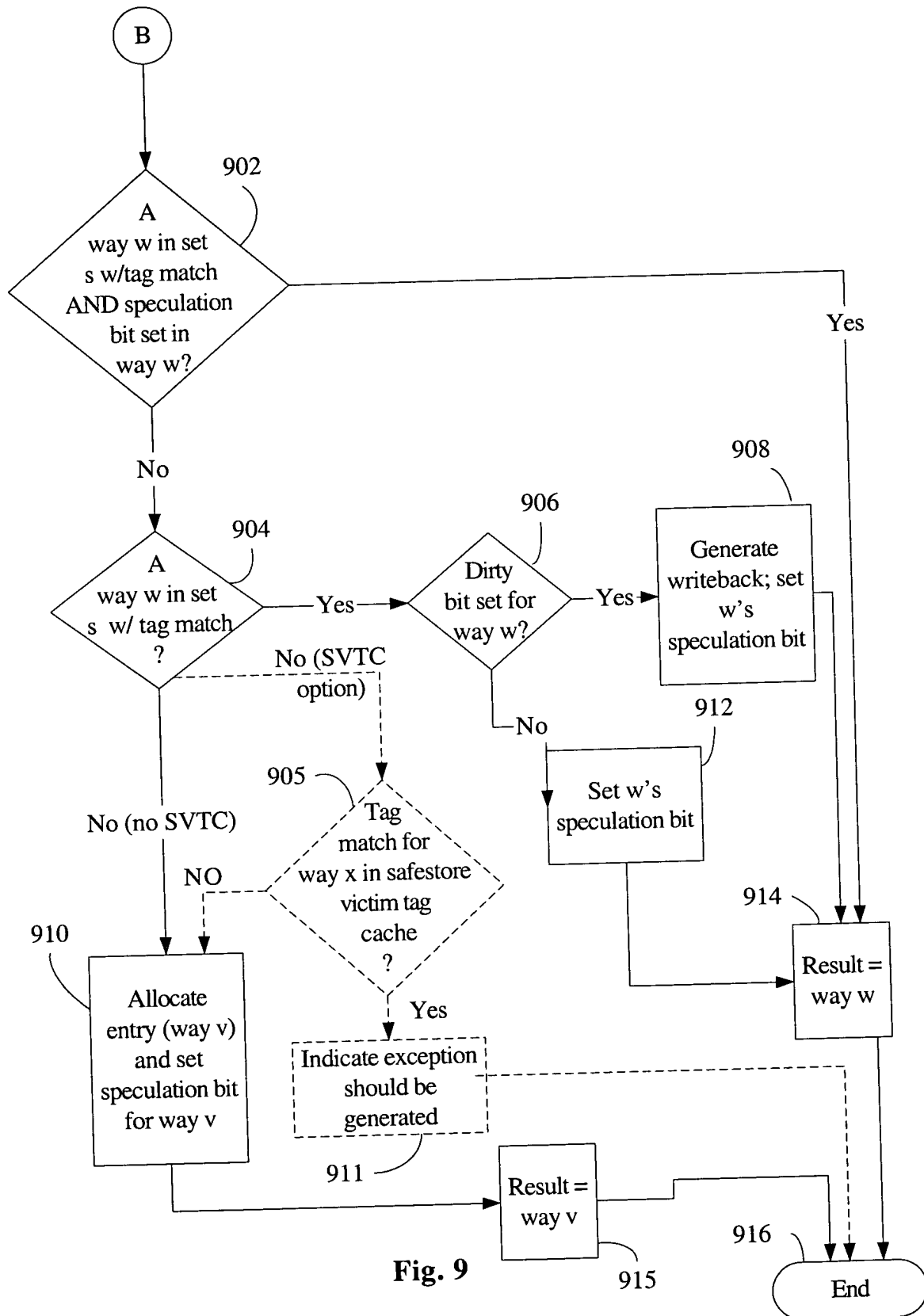


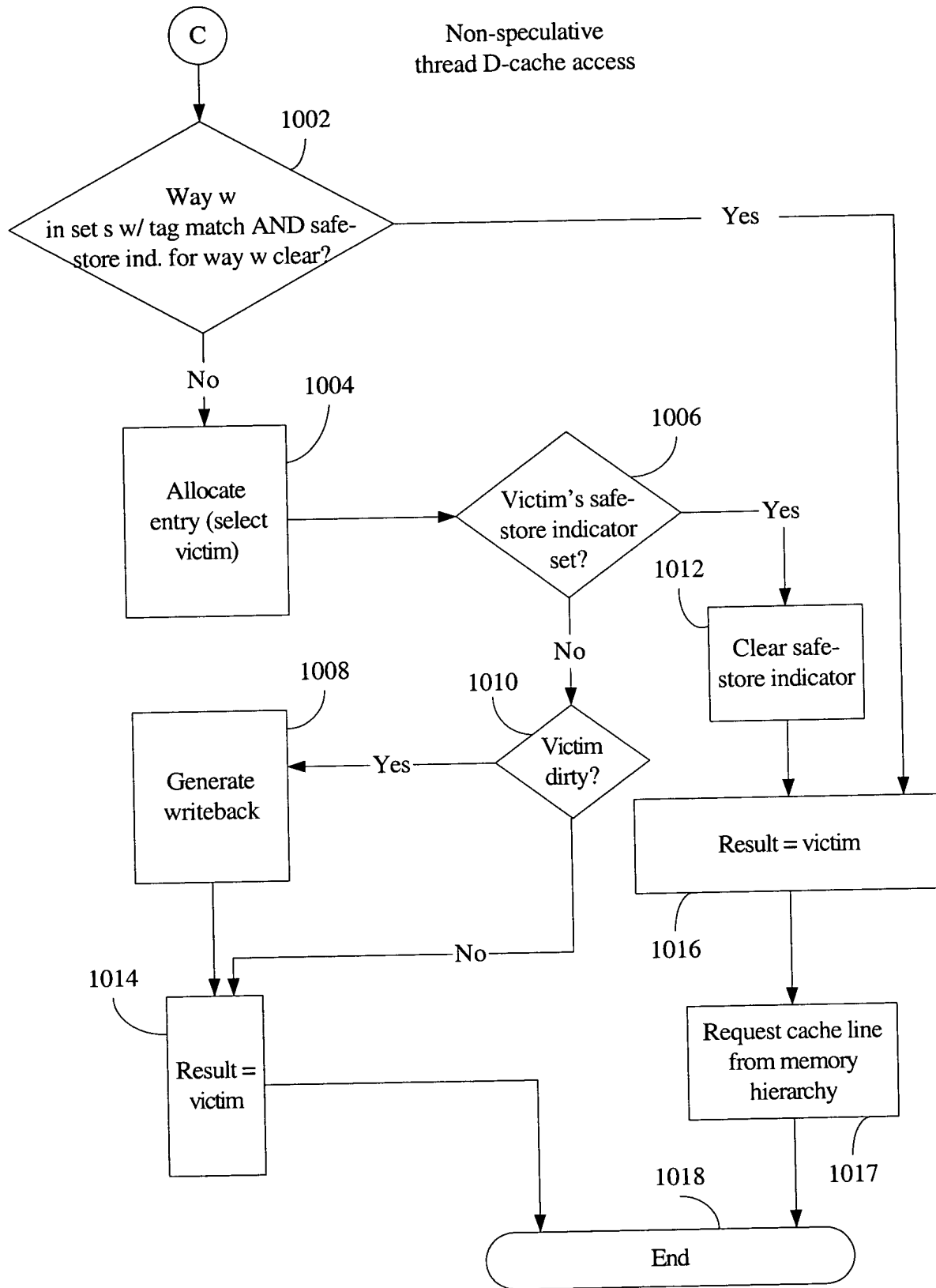
Fig. 8



# Helper thread D- cache write access



**Fig. 9**



**Fig. 10**

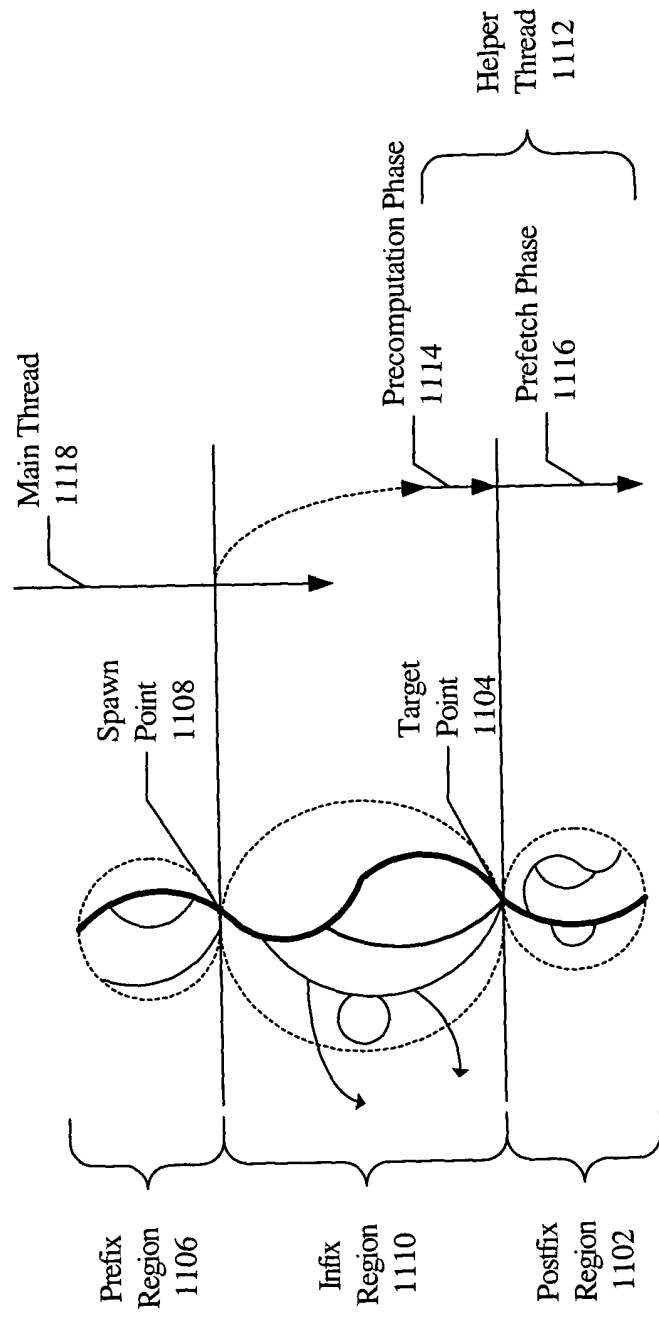
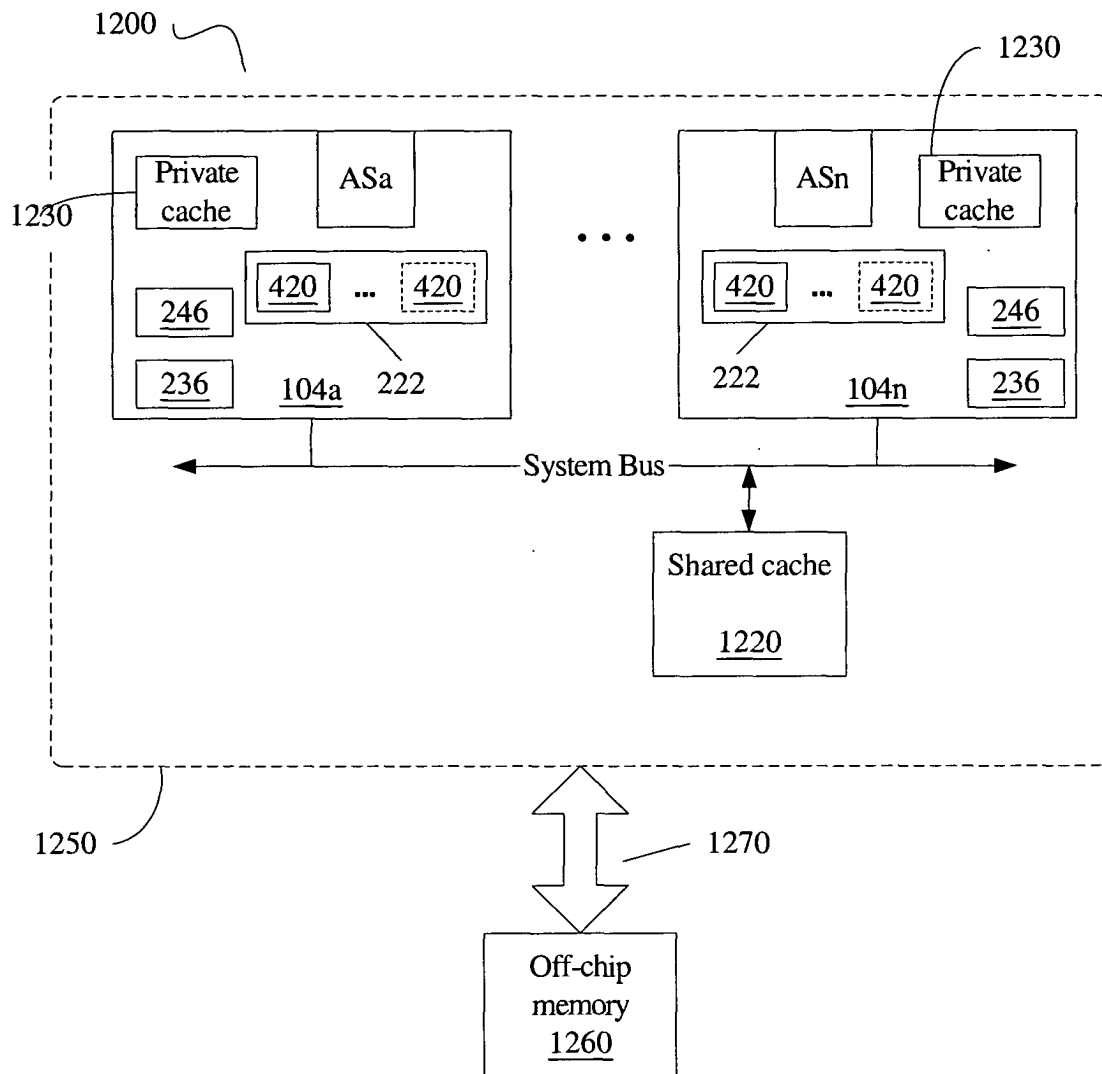


FIG. 11



**Fig. 12**